Document Title:	**Technical Note of the Integration of Adaptive Control Unit (ACU) for switched mode Power Converters**
Description:	This document describes the integration of the Adaptive Control Unit (ACU) for switched mode Power Converters
Division/ Organization:	GSI-LOEP
Field of application:	Project FAIR@GSI

Document History:

Version	Prepared by:	Checked, Date	Released, Date	Comment
V0.1	D.Schupp@gsi.de H.Welker@gsi.de Gerhard Breitenberger		17.03.2015	Pre-Release
V1.0	D.Schupp@gsi.de H.Welker@gsi.de A.Delasvecillassanchez@gsi.de			First Release

Index

1. Abbreviations and definitions

To keep this document short and well arranged, the following abbreviations are used:

ACU	Adaptive Control Unit
ADC	Analogue to digital converter
DCCT	DC current transformer
EMI	Electromagnetic interference
FPGA	Field programmable gate array
IGBT	Insulated gate bipolar transistor
ICM	Interlock & Control Module of the ACU-System
Ip	Primary current of transformer T2
LC	Inductance & capacitance (e.g. LC filter elements)
MFU	Multi-Function Unit
PI-controller	Proportional integral controller
PSS	Personal safety system (access control of the accelerator)
PWM	Pulse width modulation
Quench	Sudden transition from superconducting to normal condition
RC	Resistance & capacitance (e.g. RC filter elements)
RJ45	Registered jack (connection for telecommunication)
PSU	Power supply unit for magnet current.
SCU	Scalable Control Unit (interface between control system and ACU)
Ud1	Voltage of the DC-intermediate circuit
USI	Universal Serial Interface
19” frame	19” subrack IEC 297-3
1U	Standardized height of the electronic modules (44.5 millimeters)

2. Abstract

This document illustrates the implementation of the ACU-System into a switch mode power converter. To assure a safe operation of the power converter, the power part has to fulfill some specific demands. These demands are described in this document.

Chapter 4.3.6 lists different switch-mode topologies designed using IGBTs which will be supported by the ACU system. These topologies (clock circuits), in any case of energy recovery from the magnet, are consisting of a bridge circuit. This bridge circuit is fed from a DC intermediate circuit which includes smoothing capacitors in it. The DC intermediate circuit is supplied by a 3-phase electrical supply system over a potential-separating transformer and diode rectifier as V7 circuit (3-phase bridge circuit). The transformer sets the voltage of the intermediate circuit Ud1 according to the load demands.

The rectangular output voltage of the clock circuit varies among only the following three values:

$\{+U_{d1}; -U_{d1}; 0\}$

The frequency of the square wave voltage (e.g. 20 kHz) complies with two times of the switching frequency of the IGBT (e.g. 10 kHz). As, the arithmetic mean of this voltage depends upon the relation between the turn-on and turn-off times of the IGBTs, the clock circuit behaves like a voltage converter here.

The square wave voltage is smoothed by a LC filter and is the load voltage, which is used to control the load current in the magnet.

The control variable is the load current which is acquired, potential-free, by using a high accuracy DCCT.

The Interlock & Control Module (ICM) of the ACU-System monitors 4 analogue signals and 10 digital error-signals of the power part. The IGBT driver modules detect the error-signal through the optical inputs. In case of an error, controller- or pulse lock is set and the power converter is shut down by the main switch. Furthermore, the ICM comprises of a PWM, which creates the optical pulses for the IGBTs out of the control voltage (of the controller output).

The MFU, along with the user interface, and the ADC Module for actual value acquisition are placed in a 19´´ frame. The communication among the MFU, the ICM and other optional ACU modules is done by a serial interface (USI). The controller parameters are selected by additional software and are saved within the MFU.

Further information on configuration and commissioning of the power converter and other devices is provided in the ACU user manual.

3. Functional Specifications of the Power Part

3.1. Overview circuit diagram for power part

The overview circuit diagram for the power part is illustrated in **Figure 1**. All the components shown here are labeled according to the terminology adopted in the wiring schematics.

For the sake of clarity, the circuit diagram is divided into 5 sections. Each one of them performs a different function (ref. **Chapter 3.3**).

Section 1: Circuit for limiting the in-rush current

Section 2: Transformer, rectifier, LC filter and capacitor discharge circuit

Section 3: Output voltage converter (clock circuit)

Section 4: Output LC filter and ground sensing

Section 5: Load choke (optional in case of lower load-inductance) and load current sensing

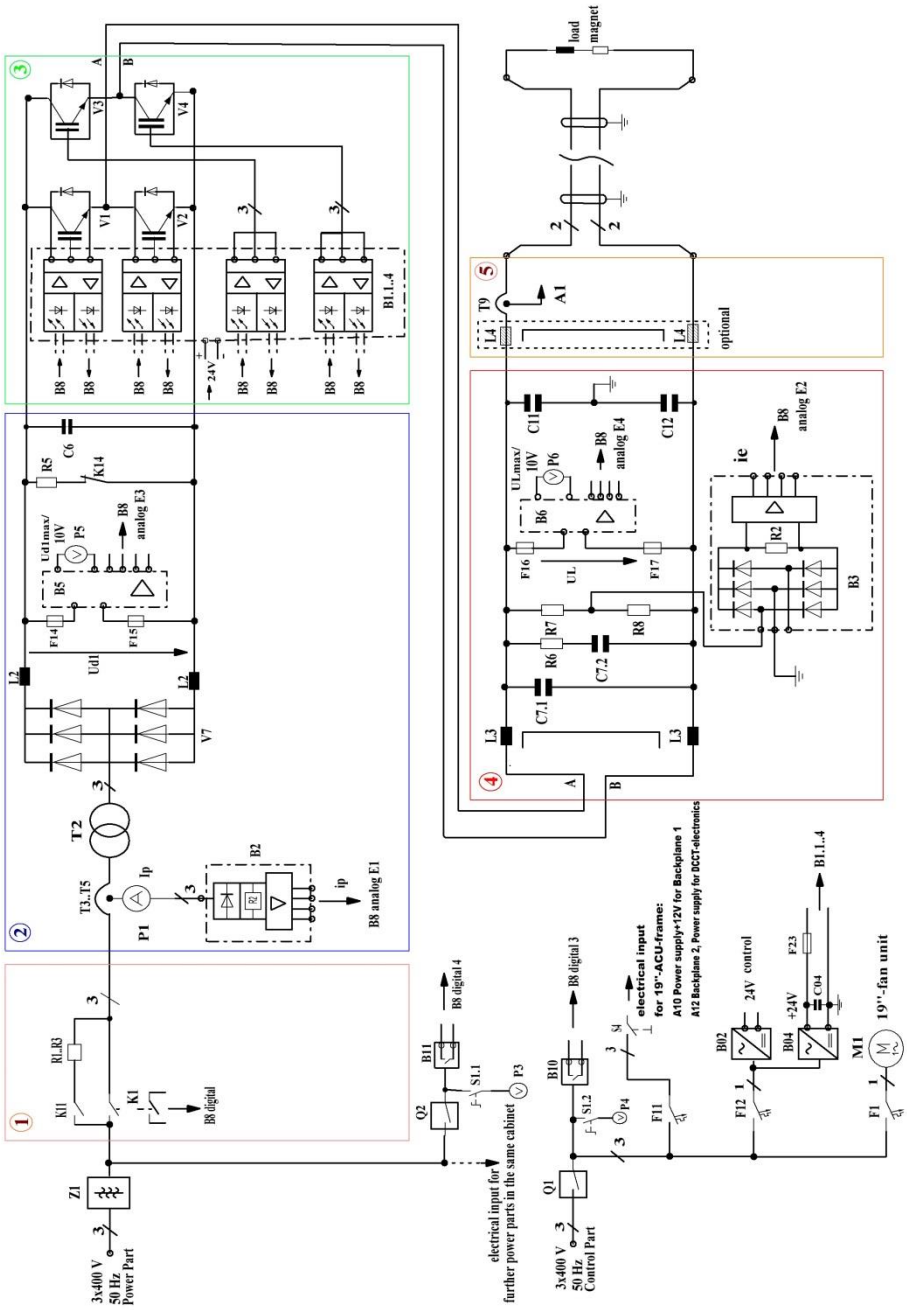

Figure 1: Overview circuit of the power part of a switched mode PSU

3.2. Component overview

Table 1 lists the components marked in the overview circuit diagram of **Figure 1**. It additionally lists the components, which are not shown in the diagram but are described in other chapters.

Components marked with "*" are a part of the ACU-System and will be delivered by GSI/ FAIR.

Remaining components are to be projected and purchased by the contractor.

If required, assembly information for the boards B1.1-4, B1.2-3, B2, B3, B5, and B6 can be provided.

Component	Name, explanation
A1*	19“ frame for the regulation & control of the ACU-System, without the boards A12-P3 und A12-P4, (ref. **Chapter 4.1**)
A10*	Single-phase voltage supply +12 V for Backplane 1 of the ACU-System, (ref. **Chapter 5.1**)
A11*	Backplane 1 of ACU-Systems, (ref. **Chapter 4.1**)
A11-P1*	Interface-card of the accelerator control system (SCU), (ref. **Chapter 4.1**)
A11-P2*	Multi-Function Unit (MFU), (ref. **Chapter. 4.1**)
A12*	Backplane 2 of the ACU-System, (ref. **Chapter 4.1**)
A12-P2*	ADC-Module 1, (ref. **Chapter 4.1**)
A12-P3	DCCT-card, (ref. **Chapter 4.1**)
A12-P4*	Three-phase DCCT-power supply, (ref. **Chapter 4.1**)
B02	24 V DC-power supply for relay-control and digital electronic interlock-logging (B8)
B04	24 V DC-power supply (recommended) for IGBT-driver supply B1.1...4
B05*	Filter for three phase current supply of the 19“ frame (ref. **Chapter 4.1**)
B06	Control valve for water flow rate regulation, (ref. **Chapter 4.3.5**)
B07	Turbine-flow meter (delivers meter pulses) flow-rate monitoring (ref. **Chapter 4.3.5**)
B1.1-4	IGBT-driver, optionally use 2 different boards: B1.1-4 for V1 and V4 B1.2-3 for V2 and V3
B2	Primary current sensor
B3	Ground fault sensor
B5	Intermediate circuit voltage sensor
B6	Load voltage sensor
B8*	Interlock & Control Module (ICM) of the ACU- System (ref. **Chapter 4.3**)
B10, B11	Line voltage monitoring
C04	Capacitor ≥1µF Polypropylene for off take of error currents from the IGBT-driver
C6	DC-intermediate circuit capacitor
C7.1	Smoothing capacitor
C7.2	Smoothing capacitor (attenuator)
C11, C12	Anti-interference capacitor for load voltage
F1	1-pole automatic circuit breaker for fan M1 for 19“-cardridge ACU-System
F3	Temperature contact of cooling plate of diode-rectifier V7 (**Figure 15**)
F4	Temperature contact of cooling plate of IGBT-bridge V1...V4 (**Figure 15**)
F5	Temperature contact of damping resistor R6 (**Figure 15**)
F14, F15	Fuse terminal strip for B5
F16, F17	Fuse terminal strip for B6
F11	Protective power-switch 3-pole for feeding 19“-frame
F12	Protective power-switch 1-pole for B02 and B04
F23	Fuse terminal strip for IGBT-driver B1.1...4
K1	Main breaker

K11	Charging contactor
K12	Mini plug-in relay 24 V DC for controlling main contactor K1 (ref. to **Chapter 4.3.4** & **3.3.2**)
K13	Mini plug-in relay 24 V DC for controlling main contactor K11 (ref. to **Chapter 4.3.4** & **3.3.2**)
K14	Discharging Circuit breaker
L2	Intermediate circuit smoothing choke
L3	Output filter choke
L4	Load choke (optional)
M1	Fan motor for 19“-cardridge of the ACU-system
P1	Current sensor (moving-iron) for primary current
P3, P4	Voltage sensor 400 V AC
P5	Voltage sensor (moving-coil 10kΩ, 10V scaled to intermediate circuit voltage)
P6	Voltage sensor (moving-coil 10kΩ, 10V scaled to load voltage)
Q1	Power switch for control part
Q2	Circuit breaker for B11 (power section for monitoring the line voltage)
R1...R3	Charging resistors
R5	Discharging resistors
R6	Output damping resistor
R7, R8	Grounding resistors
S1.1, S1.2	Voltage measuring-switch
S2	Emergency power off push-button mounted at the front side (ref. to **Chapter 4.3.1**)
S3	Door control switch (bridgeable for service) of the power section (ref. to **Chapter 4.3.1**)
S4	Control switch (3-phase)
SV6	12-pole jack for monitoring magnet flow rate, magnet temperature & flow rate control magnet (ref. **Chapter 4.3.1** & **4.3.5**)
T2	Mains transformer and temperature contacts
T3...T5	Transducer
T9*	Toroid core for sensing load current
V1/V2, V3/V4	IGBT –modules
V7	Rectifier (3-phase bridge circuit)
Z1	EMI- suppressing device

Table 1: Components marked in Figure 1 and components described in other chapters

3.3. Functional specification of the power part

3.3.1. Power supply:

The PSU contains 2 separate 3-phase supplies:

● One for the control part, to allow services at the control part, while the power part feeding is turned off.

● One for the power part.

The 3-phase supply feeds the power part over EMI suppressing device Z1 (capacitors or 3-phase EMI filter). If there is more than one channel in one frame, all of them are fed by the same 3-phase supply. It also feeds the voltage sensor B11 and the voltmeter P3 via circuit breaker Q2.

The power part can be divided in four subsections. Two of them are described as follows:

3.3.2. 3-phase circuit & DC intermediate circuit

Section 1: Circuit diagram to limit the in-rush current

Section 2: Transducer, Transformer with rectifier, LC-filter and capacitor discharge circuit

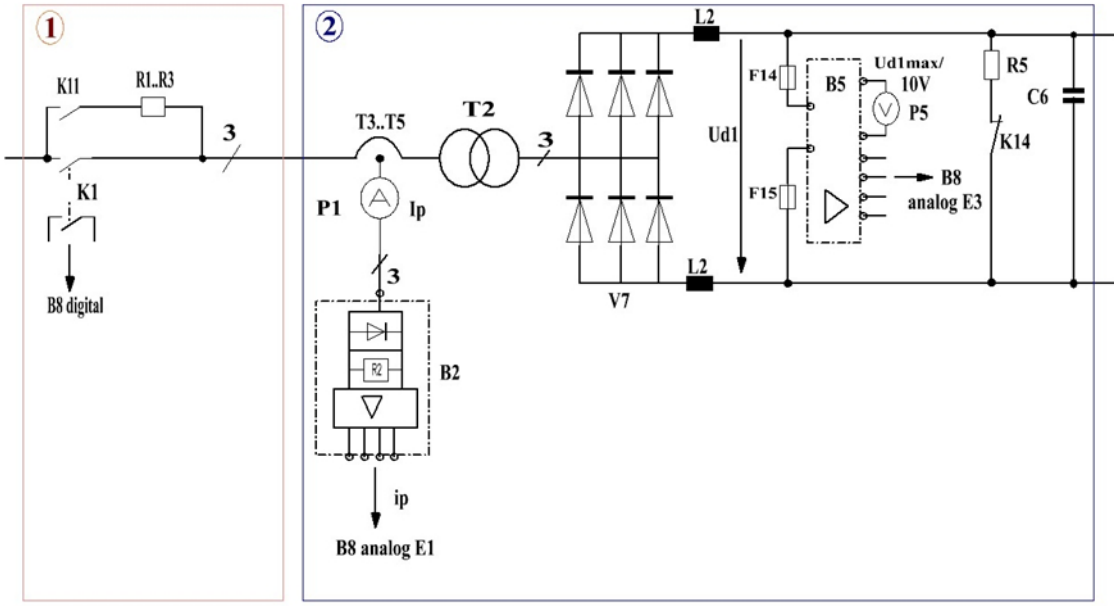

Figure 2: 3-phase circuit & DC intermediate circuit

After switching-on the equipment, the transformer (T2) is supplied via charging contactor (K11) and the charging resistors (R1, R2 and R3) to charge the DC link capacitor (C6) via the rectifier (V7) and the choke (L2). The controller is blocked and the load voltage is set to zero. After a certain duration (called “bank charging time”), the main-circuit-breaker switch K1 bridges the charging resistors. It is followed by an additional pre-set duration (“control block”) in which the controller is released and, via the “clock circuit” actuator, current is adjusted as per the applicable set value.

After switching-off the equipment, its powering back is prevented during a specified time called "power-off time". These 3 periods, bank-charging, control-block and power-off times, are a part of the parameter settings of the "Controller Parameters" that are to be set with the graphical user interface of the ACU System. The following table contains the typical time settings:

"Bank-charging time"	"Control block"	"Power-off time"
4 to 6 s	2 s	6 s

The power-off command is followed by the blocking of the controller and the switching-off of the two 24 V relays K12 (K12 switches the main circuit breaker K1,) and K13 (K13 switches the charging contactor K11 and the discharging circuit breaker K14). Further, the discharging circuit breaker K14 drops and discharges the capacitor C6 through the discharging resistor R5.

After the controller block assures that the bridge is controlled to 0, the load experiences a freewheel decay in current. Along with the controller block, the intermediate circuit current also reduced to 0. When the main circuit breaker K1 opens, the primary current is already reduced to 0.

The 3 primary currents of the transformer T2 are sensed by the 3 transducers T3, T4 and T5, rectified in the circuit board B2 and terminated by a 100 Ω load resistor. This load current is amplified by a factor of 1 in the circuit board B2 via an uncoupling amplifier and fed as the measured value i_p into the control unit E1 of the ICM (refer to **Chapter 4.3.3**).

If the i_p exceeds its threshold, which is adjusted on a plug-in module on the ICM, the PSU will be switched off with the error message of "i_p>".

The transducers have to be designed for a secondary nominal current of 100 mA. The calculated average of i_p at a given nominal primary current of transformer can be seen in the following example (voltage drop at the rectifier on B2 is not considered).

Nominal primary current from T2 transformer	Transducer ratio (for T3,T4 and T5)	Measured value of ip
23 A	50 A : 0.1 A = 500	23/ 500/ 0.817*100 = 5.6 V

The intermediate circuit voltage-sensing of circuit board B5 is in parallel with the intermediate circuit capacitors C6. The intermediate circuit voltage is reduced in circuit board B5 by a voltage divider. The first output pin feeds the voltmeter P5 on the front side of the PSU. Via an uncoupling amplifier and the second pin the measured signal Ud1 is provided to the analogue survey input (refer to **Chapter 4.3.3**) and can be used for controller-correction and overvoltage monitoring.

At the selected input nominal voltage, the voltage divider delivers 10 V at its output. The design parameters of the voltage dividers are provided in the following table:

Nominal input voltage	B5.output.1 with P5 (10kΩ)	B5.output.2 with supply ±12V	Idle voltage Udi
250 V	10 V	10 V	194 V

3.3.3. Voltage converter

Section 3: Output voltage converter (clock circuit)

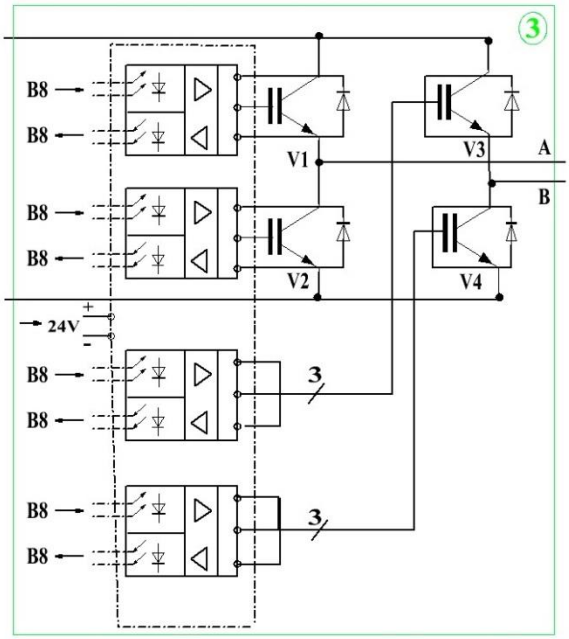

Figure 3: Voltage converter

The output voltage converter, which has been designed as a clock circuit, is the controller circuit actuator. In case of higher magnet currents it consists of 2 half-bridge IGBT transistor modules V1/V2 and V3/V4. These half bridges are wired to form a two-phase bridge circuit.

For a PSU which is designed for unipolar load current and bipolar load voltage (2-quadrant operation) the transistors V1 and V4 are controlled while V2 and V3 remain blocked (by keeping the gate emitter voltage = -15 V). In case of the negative load voltage with positive load current the magnet energy is fed back into the capacitors C6 of the DC intermediate circuit.

For a PSU which is designed for bipolar load current (4-quadrant operation) all the transistors, V1, V2, V3 and V4, are controlled. This enables both the polarities for the load voltage as well as for the load current, and, thereby, also supports in recovering the magnet energy for both the directions of the load current.

3.3.3.1. Description of the control method

The following table lists and explains the terms used in the further document.

Terms, values	Explanation
t_e	Switch on time of the IGBT-transistor in µs
Δt_{e_min}	Smallest possible change of the switch on time (PWM resolution). Its value depends on the f_{Conv}, which is adjusted by the user. For f_{Conv} = 2 kHz: Δt_{e_min} = 2,55 ns, For f_{Conv} = 96 kHz: Δt_{e_min} = 211 ps
t_a	Switch off time of the IGBT-transistor in µs
t_{a_min}	Smallest possible switch off time, to avoid simultaneously switch on of V1 with V2 and V3 with V4 with additional safety times. t_{a_min} = 4,5 µs
f_v	Switching frequency of the IGBT-Transistors V1...V4
Conv	Shortcut for Converter or voltage converter
f_{Conv}	Output frequency of the clock circuit. The available range of frequencies for the clock circuit is: f_{Conv} = 2 kHz, ..., 96 kHz
a_v	Modulation amplitude of the IGBT-Transistors V1...V4
a_{Conv}	Modulation amplitude of the clock circuit
a_{Conv_max}	Highest possible modulation amplitude of the clock circuit in consideration on t_{a_min}. a_{Conv_max} = 0,91 for f_{Conv} = 20 kHz
U_{Conv}	Arithmetic mean of the output voltage of the clock circuit

Table 2: Terms explanations

Formulas:

$$t_e + t_a = \frac{1}{f_v}$$

$$a_v = \frac{t_e}{\left(\frac{1}{f_v}\right)} = 1 - \frac{t_a}{\left(\frac{1}{f_v}\right)}$$

$$a_{Conv} = \frac{\left(t_e - \left(\frac{1}{f_{Conv}}\right)\right)}{\left(\frac{1}{f_{Conv}}\right)} = 1 - \frac{t_a}{\left(\frac{1}{f_{Conv}}\right)} = 1 - \frac{t_a}{\left(\frac{1}{2 f_v}\right)}$$

$$U_{Conv} = U_{d1} \times a_{Conv}$$

(Without considering the voltage drop across the IGBT transistors).

Through pulse width control (PWM), i.e. through changing the switch-on duration at a constant frequency f_v, the arithmetic mean of the output of the clock circuit (U_{Conv}) is set as per the formulas mentioned above.

The control method used here keeps the smallest possible switch-off time t_{a_min} always within the safety limits. In this case, the maximum possible modulation amplitude a_{Conv_max} can utmost be 91% (at f_{Conv} = 20 kHz). **Figure 4** and **Figure 5** illustrate the power-on and off durations of the IGBT transistors V1 and V4 (at f_{Conv} = 20 kHz) for two scenarios.

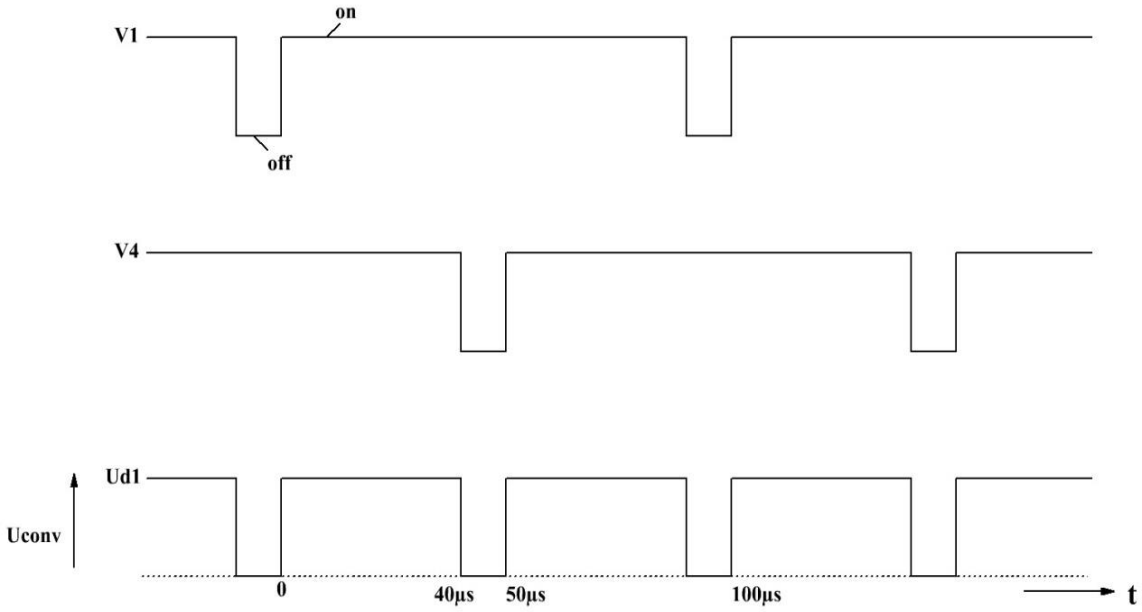

Figure 4: Transistor conduction cycle for UConv = +0.8 x Ud1

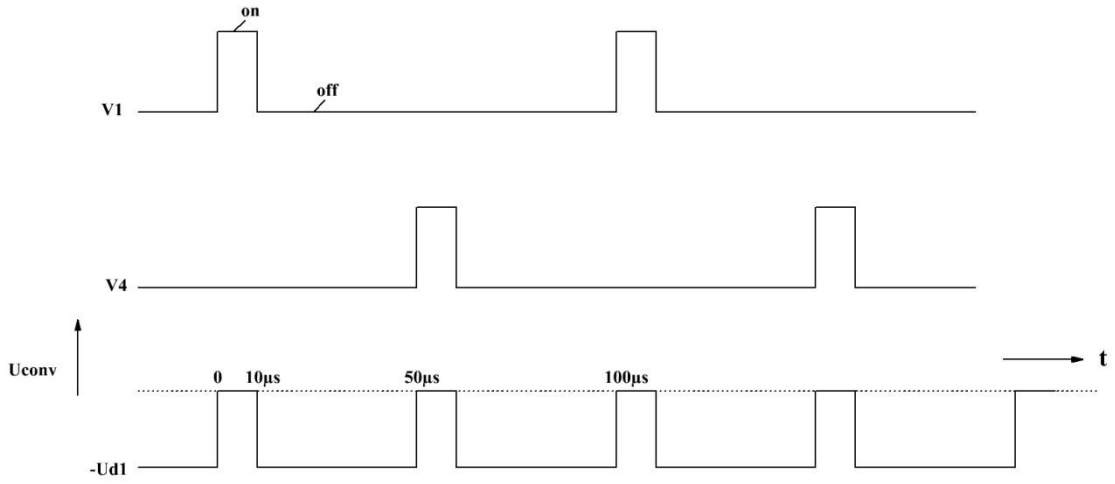

Figure 5: Transistor conduction cycle for UConv = -0.8 x Ud1

3.3.3.2. IGBT-driver

The circuit board B1.1...4 „IGBT-driver“(or two separate circuit boards B1.1-4 and B1.2-3) is connected to the gate connections and the auxiliary emitter of the IGBT transistors V1, V2, V3

and V4. Additionally, the auxiliary-collector connections are used for the desaturation monitoring, which is implemented on the circuit board as well.

In case of two separate driver circuit boards the first one (B1.1-4) drives V1 and V4 for the positive load current and the second one (B1.2-3) drives V2 and V3 for the negative load current.

For the unipolar PSUs with only positive load currents the second circuit board (B1.2-3) might be designed simpler because it needs, for the blocking of V2 and V3, only to deliver -15 V consistently.

There are only 2 signal levels (+/- 15 V) for the gate pulses.

+15 V switches the transistor on,

-15 V switches the Transistor off.

The IGBT driver switching-commands are transmitted via fiber optics from the ICM (ref. **Chapter 4.3.6**).

Light-transmission:

ON, indicates: gate-voltage +15 V, transistor on

OFF, indicates: gate-voltage –15 V, transistor off.

In the case of a transistor- or driver error the activation is carried out from the driver circuit board via fiber optics to the ICM (refer to **Chapter 4.3.2**). Light-transmission

ON, indicates: driver Ok

OFF, indicates: driver error.

The driver circuit boards are preferably supplied from a separate, common for all driver circuit boards, +24 V grounded DC voltage (B04, see **Figure 1**).

To avoid disturbances of the 24 V supply by the clock operation, the potential separation to the power part of the IGBTs has to possess a low capacitance.

Other supply voltages are also feasible, if the disturbances could be avoided within the IGBT-driver circuit.

3.3.4. Output LC filter and ground fault sensing

Section 4: Output LC filters and ground fault sensing

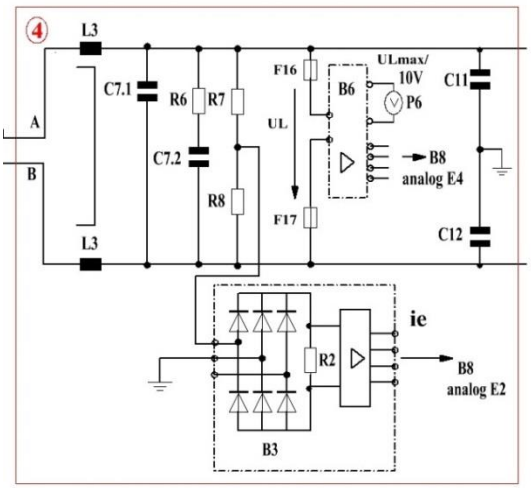

Figure 6: Output LC filter and ground fault sensing

The output ripple of the clock circuit is smoothened by a damped passive filter. The filter comprises the smoothing choke L3, capacitors C7.1 and C7.2 and the resistor R6.

The load voltage, which is isolated in potential from the line voltage, has a galvanic ground reference via the resistors R7 and R8 and the ground fault sensing B3.

In case, there is no unidirectional leakage resistance between positive or negative load rails and ground, the load voltage is maintained to ground. It means that half of the load voltage is applied between the positive load rail and ground and the other half is between the negative load rail and ground.

In the event of leakage resistance or a full ground fault between one of the load rails and the ground, a leakage current flows. This will be detected by the circuit board B3.

For both of the ground fault scenarios, voltage at the load resistor is positive and proportional to the leakage current. The downstream unity-gain isolating amplifier provides the measured value of the ground-fault current, which flows to the analogue monitoring input E2 of the ICM (ref. **Chapter 4.3.3**).

If the threshold adjusted by a potentiometer on a plug-in module of the ICM exceeds, the PSU will switch-off with the error message ie>. In case of a ground fault in the load cable or the load magnets the ground fault current is limited by the resistor R7 or R8.

Note:

Even if there is a ground fault, the PSU can still be operated without influencing the beam operation. In urgent cases, operation can be continued, by bridging analogue interlock E2 on the ICM, until there is a chance to locate the ground fault. This entails the risk of short-circuiting of load rails in case of an additional ground fault on the other rail.

Capacitors C11 and C12 serve as a capacitive ground reference and also support in dissipating the interfering-currents. This creates dynamically a ground-symmetrical load voltage as well for the high frequency noise pulses.

The “load voltage sensing” of the circuit board B6 is connected in parallel with the filter capacitor C7.1. The load voltage is reduced by a voltage divider on the circuit board B6. The first output pin feeds the P6 voltmeter on the front side of the PSU; while the measured signal UL is fed via an uncoupling amplifier and the second pin to the analogue monitoring input of the ICM (refer to **Chapter 4.3.3**). It can also be used for oscillation sensing or for controlling purposes.

For a selected input nominal-voltage, the voltage divider delivers 10 V at its outputs. The design parameters of the voltage dividers are being provided in the following table:

Nominal input voltage	B6.Output.1 with P6 (10 kΩ)	B6.Output.2 with supply ±12V
100 V	10 V	10 V

In case of the oscillations with unacceptably high-frequencies (e.g. >1 kHz) with high amplitude of the load-voltage, caused by a device error, control oscillation or too high frequencies of the set value demand, a dc voltage value is generated. This voltage is observed by the monitoring input E3 of the ICM. If it exceeds a threshold, the PSU shuts down with an error message of “oscillation monitoring”.

3.3.5. *Load choke (optional) & load current sensing*

Section 5: Load choke (optional, applicable for small load inductance) & load current sensing

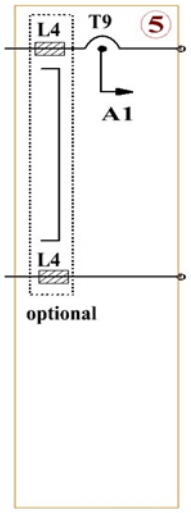

Figure 7: Load choke

The load choke L4 can be additionally applied in series with T9 before the output terminals. This enlarges the load inductance significantly and, if the magnet inductance is too small (e.g. <10 µH), reduces the current ripple.

In PSUs, which are using the load choke L4 to increase the load inductance artificially, there are two circuit boards (B6.1 and B6.2) for the load-voltage sensing. B6.1 is in parallel with the filter capacitor C7.1. Its only task is to feed the analogue monitoring input E3 of the ICM (oscillation monitor). The circuit board B6.2 captures the actual load voltage behind the load choke L4 and feeds it to the first pin of the P6 voltmeter on the front side of the PSU.

The load current I_{actual} is measured by the potential free high-precision DC current transformer (DCCT) measuring system. Its output is an analogue measured value which is normalized to ± I_{actual_max} = ±10V.

Figure 8 illustrates the functioning of the measurement system. It is PIN-compatible with Backplane 2 (A12, Table 3) and consists of three components:

● The measuring head T9 (toroid core).

● DCCT-card A12-P3: the card, along with the toroid core and the connection cable, creates a unit calibrated by the manufacturer.

● A12-P4 supplies the ± 24 V of power for DCCT-card A12-P3. As supply 3 x 400 V AC is intended.

The measured analogue value provided by the DCCT-card is fed via Backplane 2 (A12) of the ACU-System to the ADC Module 1 (A12-P2), which converts it further to the digital value.

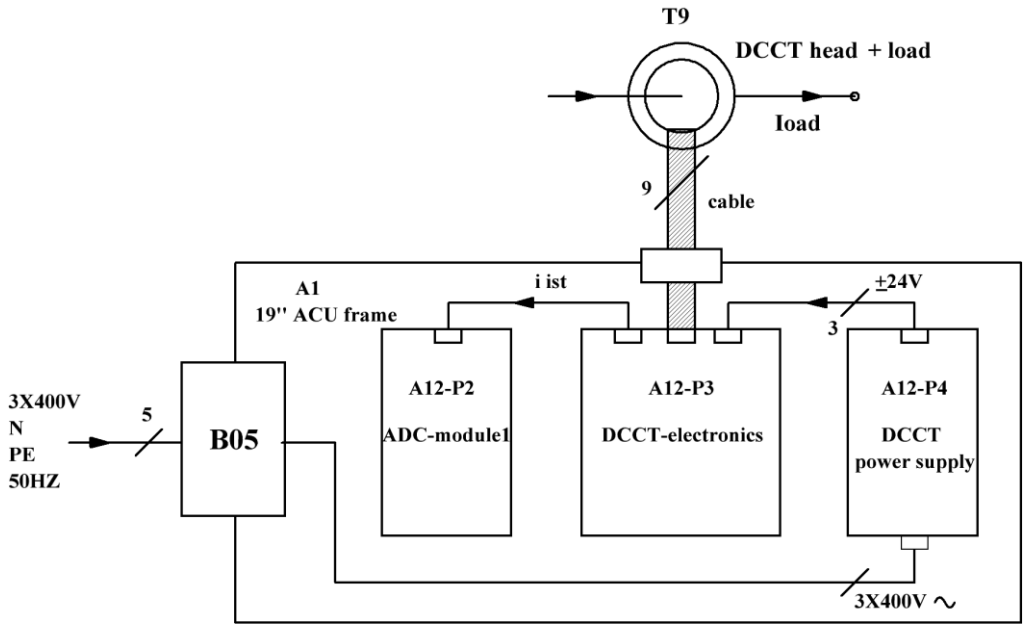

Figure 8: Functioning scheme for the Load current sensing

The company will provide the DCCT. Its rated value (current) might be higher than the nominal load current of the PSU to reduce the number of different DCCT types.

The scaling to the PSU nominal current happens in the MFU, card A11-P2 (on Backplane 1 of the 19" frame).

The pin assignment of the cards A12-P4 and A12-P3 of measuring system can be seen in Table 3.

PIN	Notation	I/O	Description
Z2	DCCT head		(via L101 to 5/X101)
Z4	DCCT head		(at 7/X101)
Z6	+24V		+24 V voltage supply
Z8	-		Not used
Z10	-		Not used
Z12	-		Not used
Z14	GNDA		Analogue ground
Z16	-		Not used
Z18	-		Not used
Z20	GNDA		Analogue ground
Z22	GNDA		Analogue ground
Z24	-		Not used
Z26	DCCT head		(at 8/X101)
Z28	-24V		-24 V voltage supply
Z30	DCCT head		(at 1/X101)
Z32	DCCT head		(at 3/X101)
PIN	**Notation**	**I/O**	**Description**
D2	DCCT Head		(at 6/X101)
D4	DCCT Head		(at 7/X101)
D6	+24V		+24 V voltage supply
D8	-		Not used

D10	PMI	I	Input for plug survey (+5V) (at ABC10/X2)
D12	PMO	O	Output for plug survey (at ABC11/X2)
D14	GNDA		Analogue ground
D16	-		Not used
D18	-		Not used
D20	GNDA		Analogue ground
D22	Analogue Signal	O	Analogue output signal from DCCT head (at ABC24/X2)
D24	-		Not used
D26	DCCT head		(at 8/X101)
D28	-24V		-24 V voltage supply
D30	DCCT head		(at 2/X101)
D32	DCCT head		(at 4/X101)

Table 3: Pin assignment of backplane 2

4. Integration of the ACU-System

4.1. Design and connection of the 19" frame of the ACU-System

Most modules and backplanes are installed in a 19" frame. This ensures simple handling of the whole system.

The 19" frame has a 3U (enclosure according to DIN 41494/IEC 297).

Figure 9: The 19" frame

The two mandatory main parts of the ACU system are the following:

● A 19" / 3U frame which is mounted on the front side of the PSU (contains MFU, ADC, back-planes and voltage supplies).

● The ICM circuit board: It is mounted at an easily accessible place in the PSU-frame and is connected to the central controlling unit via USI.

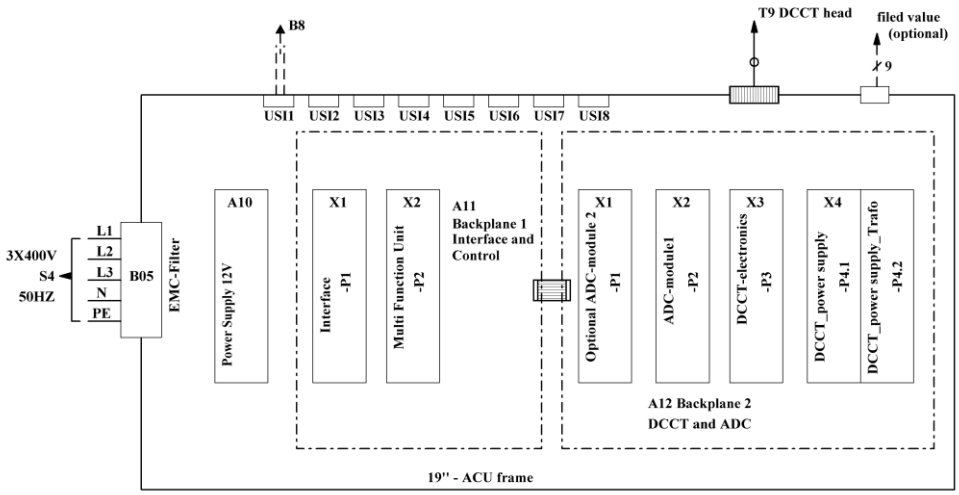

Figure 10: Principle construction of the 19“/ 3U frame of the controlling unit of the ACU-System

The A10 plug-in card is the“12 V DC Voltage Supply” of the Backplane 1. All the voltages for the Backplane 1 are generated by this supply unit.

The 3-phase supply of the S4 switch, of the PSU, is connected via the B5 EMC-filter located on the back side of the 19” frame. It feeds the DCCT power pack transformer of the card “DCCT Power Supply” A12-P4.

The MFU is the central device of the ACU-System. It is plugged on the Backplane 1 (A11) and the main tasks that it fulfils are:

● Digital control of the PSU.

● The serial communication with other devices, e.g. ADC Module, Interface card for the accelerator control system and the ICM.

● User interface for manual operation of the PSU.

Up to eight USI ports are available on the back side of the 19” frame. USI 1 is reserved for connecting the ICM. The remaining USI ports are intended for further peripheral modules. All of the unused USI ports have to be equipped with a strapping plug to bridge the interlock trip line, which otherwise would provoke an error.

If only one control variable is needed, on Backplane 2 (A12) the ADC Module 1 (A12-P1) is omitted. The insertion A12-P4 is the DCCT supply. It delivers ±24 V to the DCCT-card (A12-P3) and ±15 V to the ADC Modules 1 & 2 (A12-P1 & A12-P2).

The 15-pole connector on the back side of the 19” frame is connected to the T9 core of the DCCT. The required cable length and the connector type have to be specified when ordering the DCCT-system (comprising of the core and the circuit board A12-P3). The circuit board “A12-P4 is part of the provision of the ACU-System.

A 9-pole connector on the back side of the 19” frame accepts the optional survey of the actual field value and is connected to the optional ADC-Module 2 (A12-P1).

Except of the 3 connections shown in **Figure 10** to the PSU, there are no more connections to be established to the 19” frame from the contractor.

4.2. Digital regulation and control of the IGBTs of the clock circuit

As the IGBT has a digital regulation and control, quite highly integrated FPGA devices are used within the MFU (A11-P2) and the ICM. The Firmware and the PSU specific parameters are stored in a flash memory and it remains intact even when the supply is switched-off.

Two independent control loops with proportional and integral characteristics are available and can be cascaded. **Figure 11** shows the case of a current controlled PSU without voltage control.

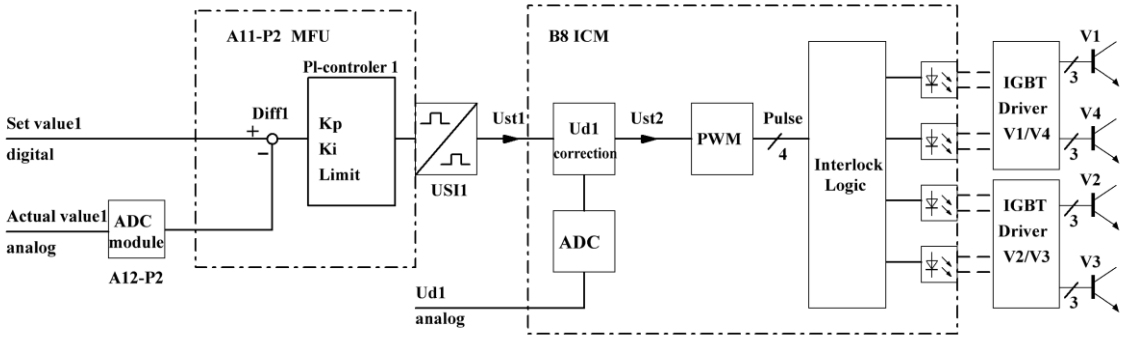

Figure 11: Block-diagram of the digital regulation and IGBT pulse-processing for the bridge circuit

The actual analogue value of the load current is sensed in the T9 DC current transformer and presented in DCCT-card (A12-P3) as a high-precision analogue value. This value is digitalized in the ADC-Module 1 (A12-P2) and send over a ribbon-cable to the MFU (A11-P2) via the Backplane 1 (A11).

The block Diff 1 calculates the control value, which is processed and limited in a PI (proportional-integral) controller as per the chosen regulation parameters (i.e. Kp or Ki) and the given regulation boundaries. This delivers the control value Ust1 and this way, the transfer function of the PI element is $F_R(s) = Kp + Ki/s$.

The control value Ust1 is sent to the ICM via USI 1 with a delay of 6 µs. If it is needed, the Ust1 can be corrected by the digitized value of the intermediate-circuit voltage, which further results in a control factor Ust2. The PWM controls the pulse-width of the transistor-activation according to the control value, however, the clock rate remains constant (e.g. 10 kHz).

When the control value is zero, corresponding to an output voltage of the clock circuit of U_{Conv} = 0 V, the switch-on and switch-off time of the transistors V1 and V4 are predetermined to be identical (refer to **Chapter 3.3.3**).

Two outputs are always electrically interlocked. So the output for V1 and V2 cannot transmit light simultaneously. The same applies to V3 and V4 as well. Further, the switch-on signal of each transistor is delayed by an adjustable delay-time t_v. This assures that two transistors of the same bridge-arm will never be connected simultaneously, which would otherwise cause a short circuit in the DC intermediate circuit. The optical driving signals are sent, for example to both of the double-IGBT-drivers, which are controlling the gate connections of the IGBT transistors.

4.3. Design and connection of the Interlock & Control Module (ICM, B8)

The ICM performs the following tasks:

● The capturing and storage of up to 10 digital-electric-error messages (e.g. temperature magnet, safety switch, mains error etc.).

● The capturing and storage of up to 8 digital-optical-error messages (e.g. transistor error).

● The capturing and limit monitoring of up to 4 analogue values of the stored signals (e.g. overcurrent i_p, line-to-earth fault etc.).

● The driving of max 4 electrical switching outputs, two of them are time wise cascaded switch-on commands for relays control.

● Output of the optical switching commands of the 4 IGBT-transistors (H-bridge) of the power section. There are maximal 8 outputs.

- The serial data-transfer over up to 4 USI connections:
  - for optional peripheral devices 2 x master-USI
  - one connection each for the 19” frame and the MFU 2 x slave-USI
- Switch-off in case of a faulty hardware trip line (independent from software)
- The triggering of interlocks (trip-line) with different security-actions in case of an error, e.g. controller-block or pulse-block.

If more monitoring inputs are required, the number of survey inputs can be increased by adding an additional and identical ICM.

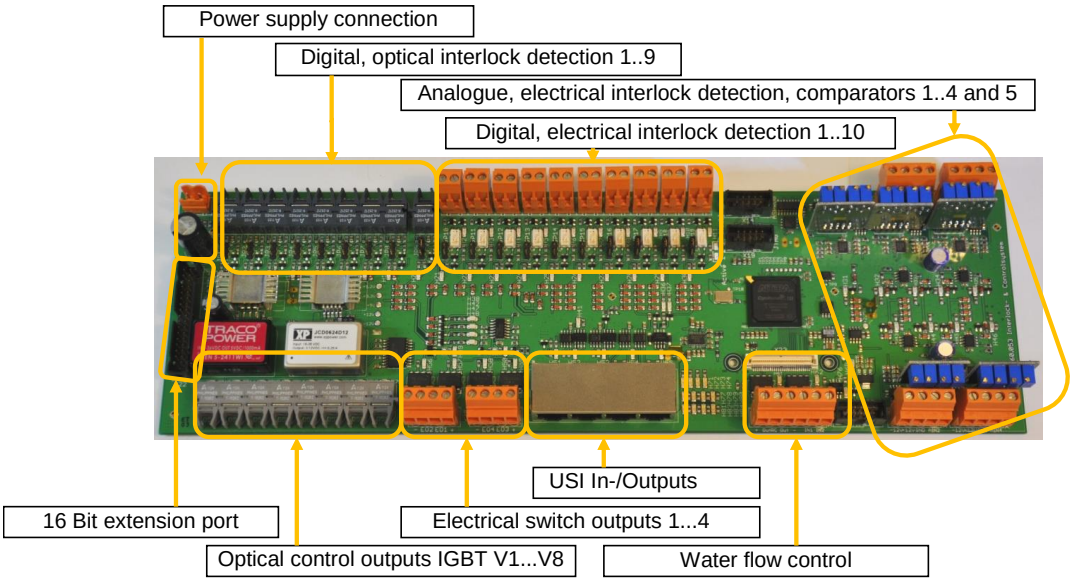

Figure 12: Interlock & Control Module

The units marked with the yellow outline are connected to the components of the power section, described in the following chapters. The ICM is supplied by the B02 supply unit. The 24 V are connected to the X1 jacket. The pin assignment is explained through the **Figure 13**.

Figure 13: 24 V Voltage supply of the Interlock & Control Module

4.3.1. Digital electrical interlock detection

The monitoring inputs are to be connected in the order shown **Figure 15**. The +24 V and ground (GND) terminal of the 24 V source (mounted over the monitoring-contact/s) are connected respectively to the first (left) and the second (right) pins of the 2-pole jacket.

The cables and the wires have to be twisted and are to be arranged to avoid any loops. The opening of the monitoring contact triggers an error in the system.

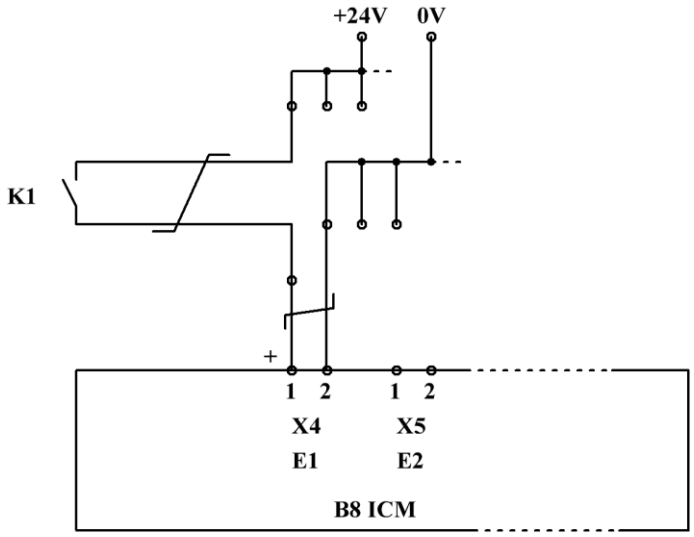

Figure 14: Wiring of the digital electrical interlock detection

Input 1 is connected to the auxiliary contact of the main breaker. It is programmed to be activated after switching-on and unlocking of the control. When the main breaker opens during operation, the PSU will be shut down with an error message. Input 7, fed over the jacket SV6 via an external contact, performs the “classic” monitoring of the magnet water flow. If the rate of flow of water in magnet is controlled, the flow-rate is captured by a turbine flow-meter. In this case, the “Water-Port” B8.X30 (ref. **Chapter 4.3.5** & **Figure 25**) is used and the input 7 is not applicable anymore. The input 8 monitors the magnet-over-temperature via an external contact which is fed by the jacket SV6 (see **Figure 25**). Input 10 is kept in reserve, but it might be used to reply for the external and optional personal-safety system (PSS)-interlocks. The appropriate programming is available.

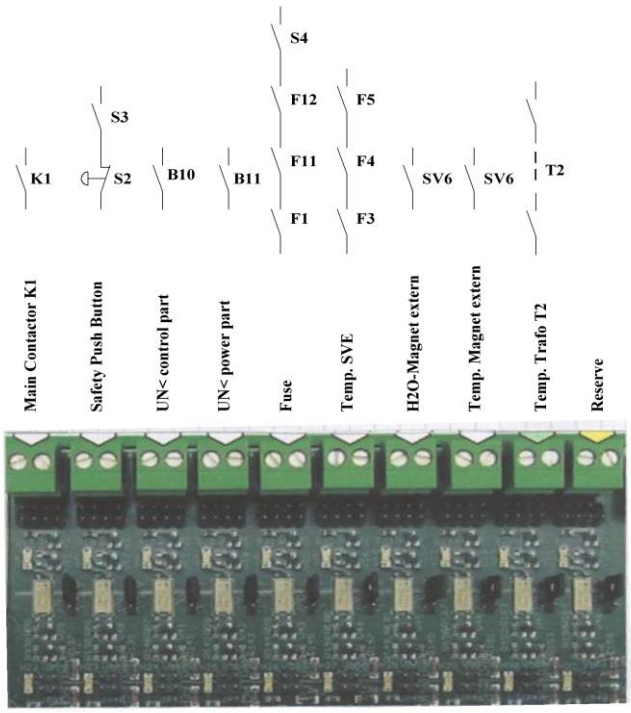

Figure 15: Digital electrical interlock detection

The controlling contacts of the power part are listed and commented in Table 4 :

Component	Name, explanation
B10	Release contact for the monitoring-device of the mains-voltage, control section (**Figure 1**)
B11	Release contact for the monitoring-device of the mains-voltage, power section (**Figure 1**)
F1	Auxiliary contact of the protective power-switch, 1-pole for fan
F3	Temperature-contact cooling-plate of diode-rectifier V7 (**Figure 1**)
F4	Temperature-contact cooling-plate IGBT-clock-bridge V1, V2, V3 and V4 (**Figure 1**)
F5	Temperature-contact of damping-resistor R6 (**Figure 1**)
F11	Auxiliary contact of the protective power-switch 3-pole (**Figure 1**)
F12	Auxiliary contact of the protective power-switch 1-pole for 24 V –supply. (**Figure 1**)
K1	Auxiliary contact of the Main breaker K1 (**Figure 1**)
S2	Safety push-button switch, mounted on the front side
S3	Door control switch (bridgeable for service) of the power section
S4	Manual controller (3-phase) for the 19“ frame (**Figure 1**)
SV6	12-pole jacket for magnet-monitoring and for flow rate control (**Figure 25**)
T2	2 x 3 temperature-contacts of the power transformer T2 (**Figure 1**)

Table 4: Controlling contacts of the power part

Inputs which are not used can be deactivated by jumpers on the ICM.

4.3.2. Digital optical interlock detection 1...8 and 9

There are 9 digital acquisitions for optical interlock sources (see **Figure 16**).

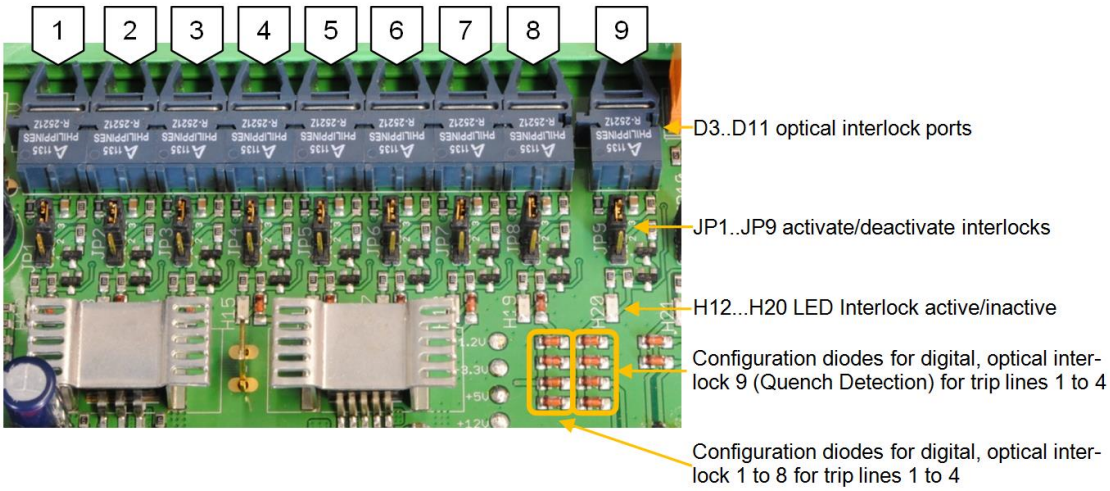

Figure 16: Digital, optical interlock acquisition

The inputs 1, 2, 3 and 4 are used for the IGBT bridge circuit (see **Figure 17**). If the remaining inputs are not used (this means without light), they have to be deactivated by placing the jumpers on the circuit board.

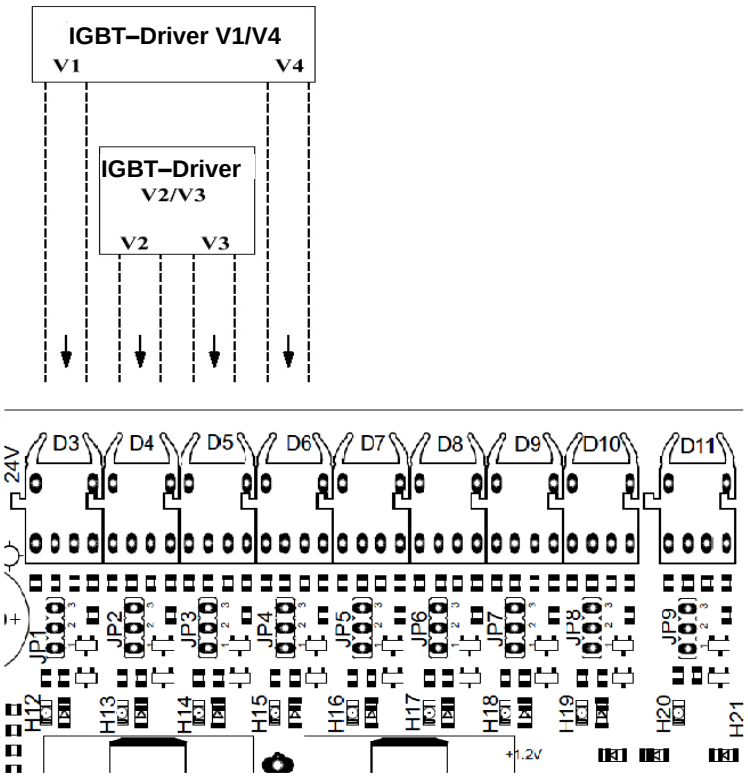

Figure 17: Digital-optical-interlock detection/ detector

The 9th input is reserved for quench-monitoring of the superconducting magnets.

The Quench detection interlock acquisition affects trip lines 1 to 4. This can be configured using 4 diodes.

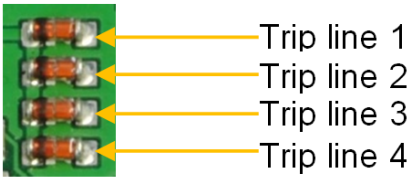

Figure 18: Trip line configuration of the Quench Detection

If those trip lines are not supposed to be used, the respective diodes have to be removed (see **Figure 16** and **Figure 18**).

4.3.2.1. Activate/deactivate interlocks

There are included jumpers to activate/deactivate the channel for digital, optical interlocks (see **Figure 16**):

- 1-2 Channel is active
- 2-3 Channel is inactive

4.3.2.2. LEDs

The LEDs H12...H20 glow in case of an error at the respective digital, optical interlock port.

4.3.2.3. Trip line configuration of digital, optical interlock acquisitions 1...8

The digital, optical interlock acquisitions 1 to 8 affect trip lines 1 to 4. They can be configured using 4 diodes.

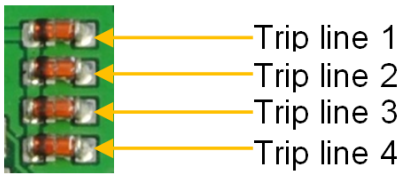

Figure 19: Trip line configuration of the digital, optical interlock acquisitions 1...8

In **Figure 19** the digital, optical interlock acquisitions 1 to 8 belong to trip lines 1 to 4. If those trip lines are not supposed to be used, the respective diodes have to be removed.

4.3.3. Analogue, electrical interlock detection

One unipolar and four bipolar comparators are used with filters to define switch threshold and response behaviour. If they are activated for interlocks, exceeding or falling below the comparator voltage will be recognised as an interlock.

The comparators are configured with plug-in filter modules. Those modules have 4 potentiometers for setting the comparator thresholds as well as a user definable RC filter.

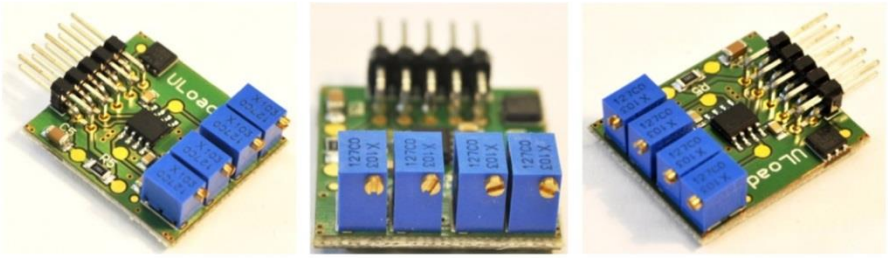

Figure 20: Plug-in filter modules of the ICM

Four analogue electrical values from the power part are monitored with these inputs. Each channel is led over a separate, analogue and user configurable, RC-filter to generate an average-value-monitoring. It is followed by a comparator with a threshold adjustable by a potentiometer. An error occurs if the signal exceeds this threshold value. The RC-filters and the potentiometers of all the four inputs are placed on plug-in circuit boards. Therefore, if the ICM has to be replaced, it is easy to keep the adjusted values by simply changing the plug-in circuit boards.

Three pins of each jacket provide additionally +12 V, -12 V and GND to supply connected monitoring modules.

The E4 analogue input for over-voltage monitoring as well as for the oscillation monitoring of the load-voltage are in parallel to C7.1 (**Figure 1**). In case, if the oscillation with unacceptably high-frequencies (e.g. >1 kHz) with high load voltage amplitude caused by device error, control oscillation or too high frequencies of the set value demand, a dc voltage value is generated. This voltage is observed. Both monitoring values are smoothed in separate plug-in modules and monitored to limits adjusted by comparators. If it exceeds those limits, the PSU is shut down with the error message “oscillation monitoring” or “load over-voltage”.

Further information regarding the adjustment and configuration of the comparators and RC-filters can be found in the ACU manual.

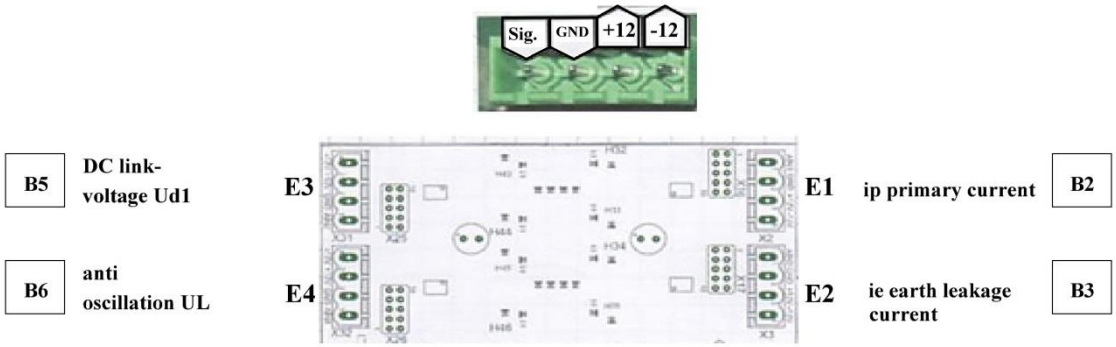

Figure 21: Analogue electrical interlock detection and connector pin-assignment7

The analogue electrical measuring values of the power part shown in **Figure 21** are listed and commented in **Table 5**:

Value	Name, explanation
B2	Actual-value of Primary-current i_p (positive DC voltage, captured in B2 circuit board "primary-current monitoring") (**Figure 1**)
B3	Earth-fault current i_e (positive DC voltage, captured in B3 circuit board "earth-fault monitoring" (**Figure 1**)
B5	DC intermediate-circuit-voltage U_{d1} (positive DC voltage, captured in B5 circuit board "intermediate-circuit voltage monitoring" (**Figure 1**)
B6	Load voltage U_L at the C7.1 filter capacitor, captured in B6 circuit board „load voltage monitoring" (**Figure 1**)

Table 5: Analogue electrical measuring values of the power part

4.3.4. Electrical switching outputs 1...4

There are 4 electrical switch outputs.

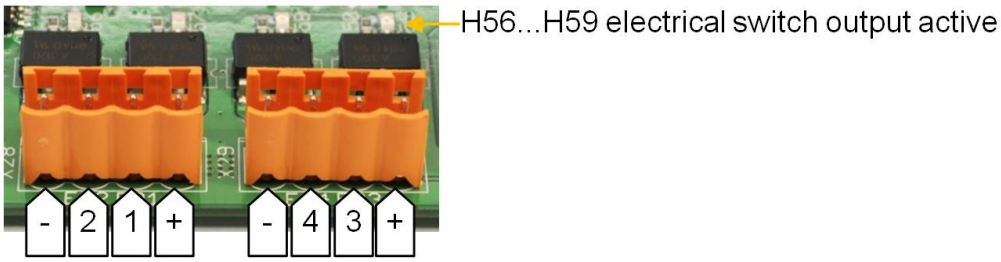

Figure 22: Electrical switch output

Each of the 4-pole jackets consists of 2 electrical switching outputs. But, normally, only two out of these 4 outputs are used e.g. at pin 2 and pin 3. Pin 1 and 4 are connected respectively to the +24 V and 0 V supply voltage terminals. The switching outputs are able to short circuit against either 0 V or 24 V.

- The first jacket X28 is used for switching on the PSU.
- Pin 2 drives the K13 24 V relays, which switches the charging contactor K11 (see **Figure 1**)
- Pin 3 switches after expiry of the "bank-load-time" the relays K12, which switches the main breaker K1 (see **Figure 1**).

If the optional personal safety system (PSS) is required, the output pin 2 of the second jack x29 is to be used for sending feedback to the PSS.

Figure 23 shows the default assignment of the switching outputs.

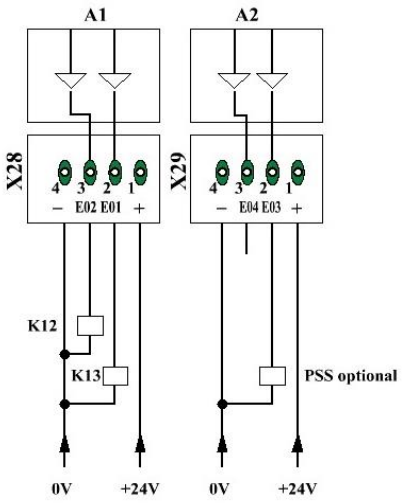

Figure 23: Electrical switching outputs

Output	Function
1	Load protection
2	Main protection
3	Personal Protection System (if PSS is active, the switch output is open)
4	External control lock (if the control is locked, the switch output is open)

Table 6: Pin assignment of the electrical switch output

4.3.5. Water flow rate: control & monitoring

The ICM contains a separate port to control water flow.

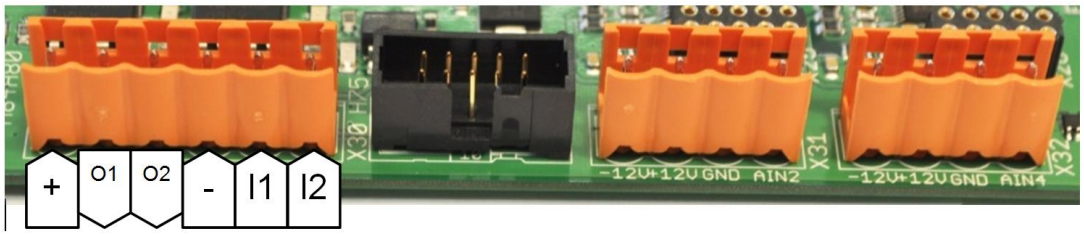

Figure 24: Water flow control

+ Power supply of the Output Schmitt-Trigger

O1 Output Schmitt-Trigger 1

O2 Output Schmitt-Trigger 2

- Power supply of the Output Schmitt-Trigger

I1 Pulse entry 1

I2 Pulse entry 2

The 6-pole jacket X30 is the interface to the water-flow-rate control, which is controlling the flow-rate for the magnet and monitoring the flow-rate for the PSU. The following components are to be connected:

● Regulating valve V_{mag} for controlling the flow-rate of the magnet (external)

● Turbine-flow-meter B07 delivers meter pulses for monitoring the flow-rate of the PSU (internal).

● Turbine-flow-meter Q_{mag} delivers meter pulses for monitoring the flow rate of the magnet (external).

Pin 1 is connected to the control voltage +24 V

Pin 4 is connected to the control voltage 0 V

Pin 2 (OutRC) delivers the delayed switching command “open” to the external regulation valve, V_{mag}, of the magnet. For this, the components of the RC-filter are not assembled. For regulation valves with analogue control voltage the RC-filter is used for smoothing of a PWM-modulated square-wave voltage. In this case Pin 3 is not used.

Pin 3 (out) delivers the switching command “close” to the external regulation valve V_{mag}, of the magnet, without a delay.

Pin 5 receives the meter pulses of the flow-meter B07 of the PSU at IN1.

Pin 6 receives the meter pulses of the external Q_{mag} flow-meter of the magnet at IN2.

The frequency of the meter-pulses is measured for the water flow-rate. If it falls below a given limit, the PSU is shut down with an error message. The processing of the meter-pulses and the regulation of the desired flow-rate is done by the FPGA of the ICM.

The assignment of the in- and outputs can be seen in **Figure 25**.

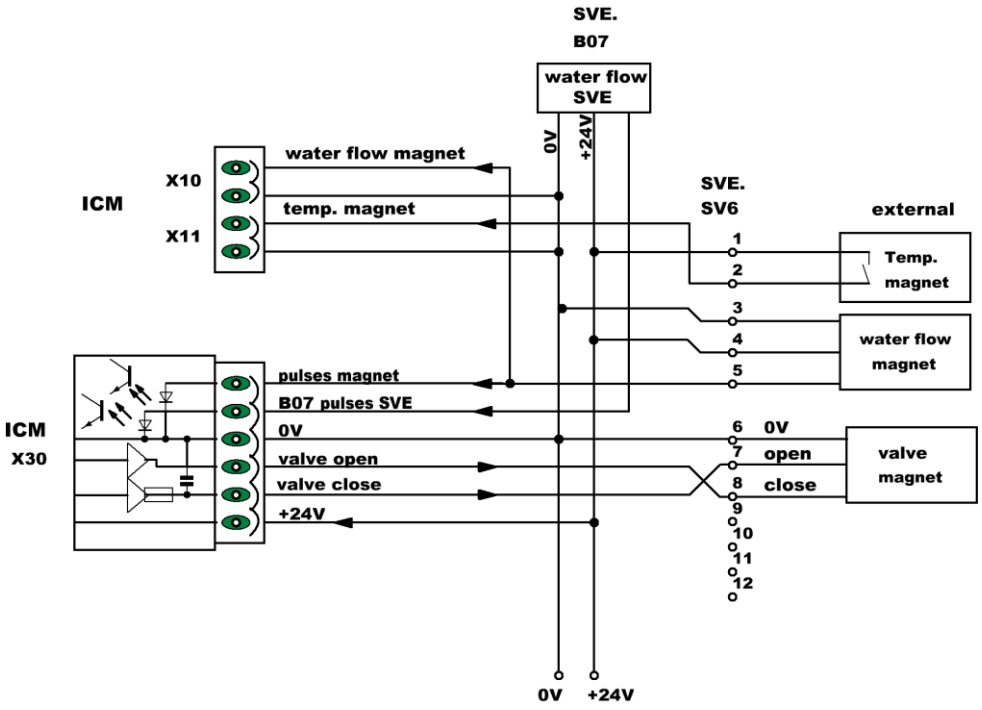

Figure 25: Controlling & monitoring of the water-flow-rate of the PSU and the magnet

The jacket SV6 is used for the transmission of the magnet flow-rate signals. It is located near the load-connectors. The assignment of different ports of the jacket can be seen in **Figure 25**.

4.3.6. *Optical outputs for the IGBT drivers*

There are 8 optical switch outputs for IGBT pulse logic.

Two outputs are electrically isolated from each other, which means that output 1 and output 2 cannot get light at the same time. This prevents 2 IGBTs of a bridge to be connected at the same time.

Figure 26 shows the assignment of the optical outputs.

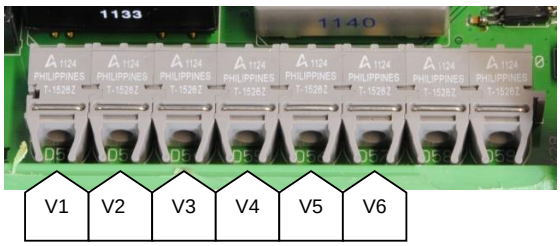

Figure 26: Pulse logic outputs for IGBTs

Although the bridge circuit with 4 IGBTs is used as standard circuit for most of the PSUs in particle accelerators, other clock-circuits are also realizable with the ACU-System.

The following chapters list further clock circuits. The IGBTs V1...V6 are driven by the pulse-outputs shown in **Figure 26**. The firmware for those clock circuits is already implemented.

The benefits and drawbacks of the different clock-circuits as compared to the standard full-wave control bridge circuit are explained in the following section.

4.3.6.1. *Clock circuit variance 1, bipolar current with energy recovery, standard circuit*

4-quadrant operation

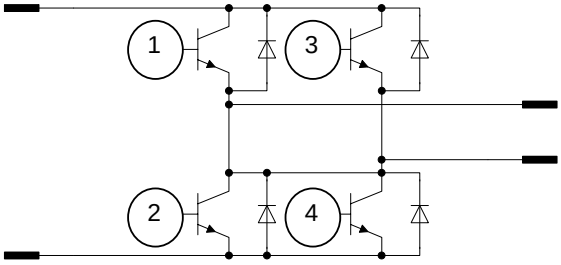

Figure 27: Assignment of the IGBTs in bipolar operation with energy recovery

Characteristics of the circuit:

- Possibility of bipolar current
- Possibility of bipolar load-voltage
- Possibility to recover the magnetic energy to the DC intermediate circuit
- The clock frequency of the IGBTs V1/V4 and V2/V3 matches to the half of the output frequency of the clock circuit. This situation leads to the lower switching losses of the IGBTs.

4.3.6.2. Clock circuit variance 2, unipolar current with energy recovery, half-wave control-bridge

2-quadrant operation

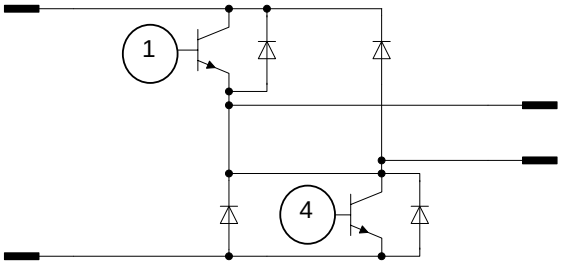

Figure 28: Assignment of the IGBTs in unipolar operation with energy recovery

Disadvantages of the circuit:

● Possibility of only unidirectional current

Advantages of the circuit:

● For V1 and V4 only one full functional driver is required. A comparatively simpler driver for V2 and V3, that pulls the gate-connector to -15 V permanently, is sufficient.

● Bipolar load voltage and hence the recovery of the magnetic energy to the DC intermediate circuit is possible

●The clock frequency of the IGBTs V1/V4 matches to the half of the output frequency of the clock circuit. This leads to lower switching losses of the IGBTs.

4.3.6.3. Clock circuit variance 3, unipolar current without energy recovery, Chopper-circuit

1-quadrant operation

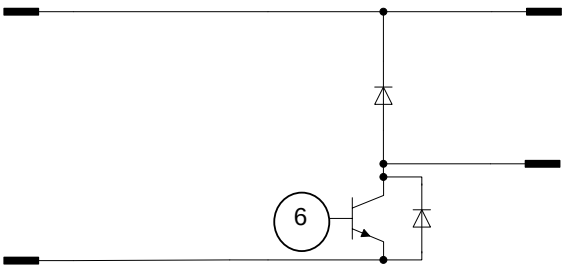

Figure 29: Assignment of the IGBTs for unipolar current without energy recovery

Disadvantages of the circuit:

● Only unidirectional current is possible

● Only unipolar load-voltage is possible; recovery of the magnetic energy to the DC interme-diate-circle is not possible

● Very low load voltages are not possible, because the switch-on time of V6 cannot be shorter than a certain limit

● Clock frequency of the IGBT V6 corresponds with the output frequency of the clock circuit.

Advantages of the circuit:

● Simple constructional design

● Forward power loss of the IGBT is halved as compared to the full wave bridge

This circuit requires a different configuration of the PWM than the bridge circuit mentioned in **Chapter 3.3.3.1**. This can be chosen from a drop down menu in the configuration software. With a control value of 0, what equates the output voltage of the clock circuit U_{Conv} = 0 V, the switch-on time of the V6 transistor is 0, respectively a minimal but still realistic value.

4.3.6.4. Clock circuit variance 4, bipolar current with reversible capacitor-bank (Kicker)

PSUs for very fast rising currents with controlled DC-periods can use the clock-circuit shown in **Figure 30** with 6 IGBTs. Similar to the standard circuit, this circuit is also bipolar for both the load-voltage and the load-current.

For a sharp current rise, V5 is switched-on while V6 is switched-off. This way, the higher intermediate-circuit voltage gets connected to the load.

For the duration when the DC-current flows, V5 is switched-off while V6 remains on. This way the low voltage intermediate-circuit gets connected to the load and it makes the DC-current operation possible. This condition leads to the reduced switching losses of the IGBTs V1, V2, V3 and V4.

4-quadrant operation

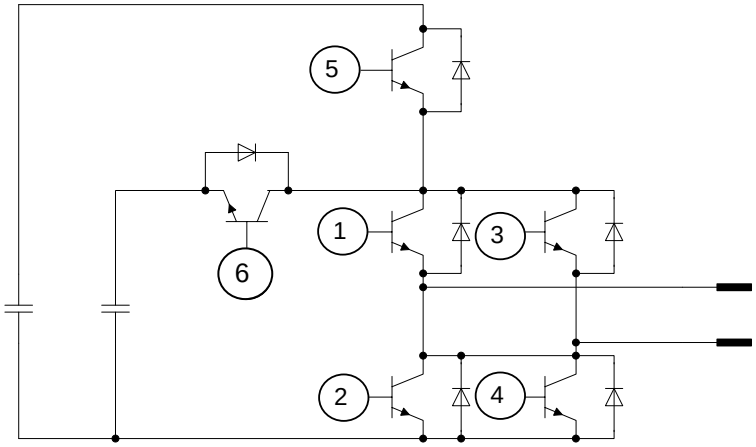

Figure 30: Configuration of the IGBTs for the bipolar operation with energy recovery and reversible capacitor-banks of the 2 DC intermediate-circuits

4.3.7. USI ports

There are 4 USI ports (RJ45) on the ICM (see **Figure 31**).

2 x master-USI (M1 & M2): For optional periphery-modules

2 x slave-USI (S1 & S2): One for the interconnection to the 19“frame and the other one for the MFU (host).

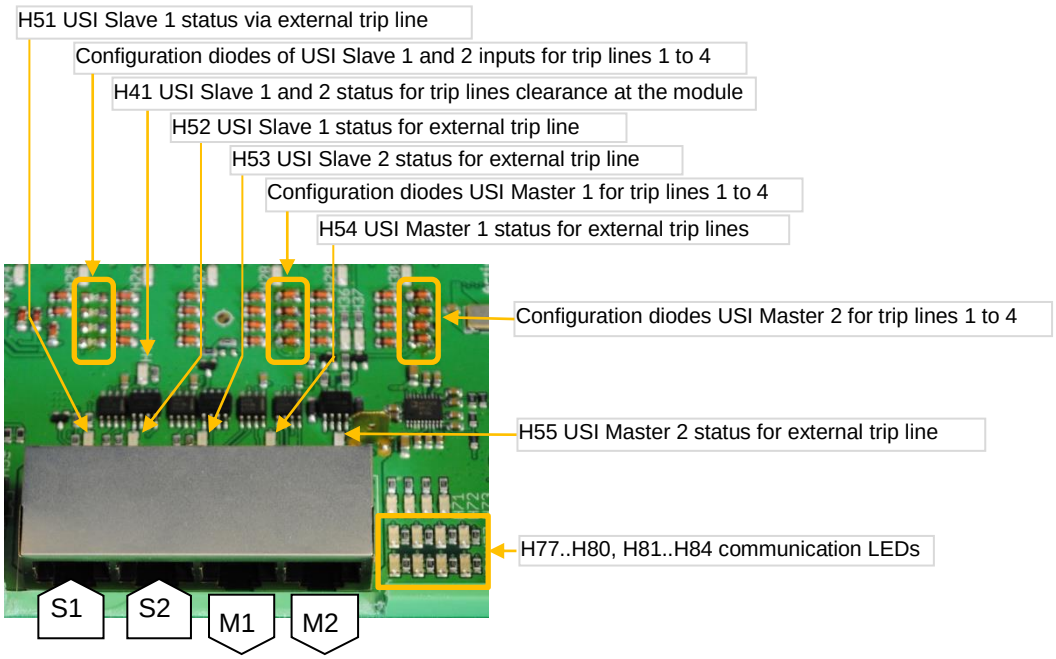

Figure 31: Master and slave USI In-/Outputs (RJ45) on the ICM

All of the unused USI ports must be equipped with a trip-line-bridge.

4.3.8. Connections and interfaces

All electrical connections of the ICM are done via multi-pin connectors, type Phoenix Contact Series MSTBVA, pitch 5.08mm.

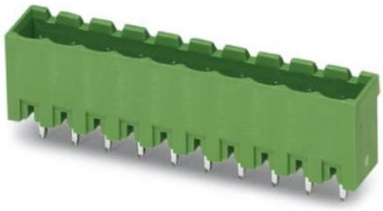

Figure 32: 10-pol version of the Phoenix multi-pin Series MSTBVA

All optical connections of the ICM are done via AVAGO Series HFBR-0500Z plugs. The AVAGO Series HFBR-0500Z – R2521Z requires a light signal via optical fiber cable. If the signal is interrupted and the port is active, this will be recognized as an interlock.

Figure 33: Example for plugs of the AVAGO Series HFBR

4.3.9. 16 Bit expansion port

This multi-pin connector is used to connect an expansion module to the ICM for additional functions. For example, to increase the number of interlock ports or outputs for additional control pulses or signals.

Figure 34: 16 Bit Extension port

PIN	Description	I/O	Explanation
1	Trip line 1	I	Trip line 1
2	GND		Ground
3	Trip line 2	I	Trip line 2
4	GND		Ground
5	Trip line 3	I	Trip line 3
6	GND		Ground
7	Trip line 4	I	Trip line 4
8	ID	I/O	1-wire ID
9*)	Trip line Pull-up Supply	O	+5 Volt DC for Trip lines
10*)	Trip line Pull-up	I	Head point of the Trip line resistors
11	Trip line Status 2	O	Status of trip line 2 is stored using a hardware flip-flop
12	Switched 5V_1	O	Status of trip line 1 is stored using a hardware flip-flop
13	+5 Volt	O	+5 Volt DC output
14	+5 Volt	O	+5 Volt DC output
15	+12 Volt	O	+12 Volt DC output
16	-12 Volt	O	-12 Volt DC output
17	GND		Ground
18	GND		Ground
19	Extension Bus 0	I/O	Bus wire from/to FPGA
20	Extension Bus 1	I/O	Bus wire from/to FPGA
21	Extension Bus 2	I/O	Bus wire from/to FPGA
22	Extension Bus 3	I/O	Bus wire from/to FPGA
23	Extension Bus 4	I/O	Bus wire from/to FPGA
24	Extension Bus 5	I/O	Bus wire from/to FPGA
25	Extension Bus 6	I/O	Bus wire from/to FPGA
26	Extension Bus 7	I/O	Bus wire from/to FPGA
27	Extension Bus 8	I/O	Bus wire from/to FPGA
28	Extension Bus 9	I/O	Bus wire from/to FPGA
29	Extension Bus 10	I/O	Bus wire from/to FPGA
30	Extension Bus 11	I/O	Bus wire from/to FPGA

31	Extension Bus 12	I/O	Bus wire from/to FPGA
32	Extension Bus 13	I/O	Bus wire from/to FPGA
33	Extension Bus 14	I/O	Bus wire from/to FPGA
34	Extension Bus 15	I/O	Bus wire from/to FPGA

*) Pins 9 and 10 have to be connected by a short-circuit bridge, if no expansion module is present, to disable the trip lines to the expansion module. Otherwise it is not possible to delete or acknowledge those trip lines.

Table 7: Pin assignment of the 16 Bit extension port